Synopsis V1.0
Single Event Effects Testing of the Texas Instrument TLK2711 Transceiver

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I. Introduction

This study was undertaken to determine the single event destructive and transient susceptibility of the Texas Instrument TLK2711 Transceiver. The device was monitored for transient interruptions in the output signals and for destructive events induced by exposing it to a heavy ion beam at the Lawrence Berkeley National Laboratory's Berkeley Accelerator Space Effects Facility (BASEF).

II. Devices Tested

The TLK2711 is a member of the WizardLink transceiver family of multigigabit transceivers, intended for use in ultrahigh-speed bidirectional point-to-point data transmission systems. The TLK2711 supports an effective serial interface speed of 1.6 Gbps to 2.7 Gbps, providing up to 2.16 Gbps of data bandwidth.

The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector terminals, and transmit/receive terminals. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. It is then reconstructed into its original parallel format. It offers significant power and cost savings over parallel solutions, as well as scalability for higher data rates in the future. The TLK2711 performs data conversion parallel-to-serial and serial-to-parallel. The clock extraction functions as a physical layer interface device. The serial transceiver interface operates at a maximum speed of 2.7 Gbps.

The transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (TXCLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit (8b/10b) encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (TXCLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the recovered clock (RXCLK). It then decodes the 20-bit wide data using the 8-bit/10-bit decoding format resulting in 16 bits of parallel data at the receive data terminals (RXD0-15). The outcome is an effective data payload of 2 Gbps to 2.5 Gbps (16 bits data x the frequency).

The sample size used during the tests was two. The devices were manufactured by Texas Instrument and were characterized prior to exposure. The devices tested had a Lot Date Code of 0545. All DUTs' package markings were identical and are given in the table below:

XTLK2711
THA
5DAC0545Q

III. Test Facilities

Facility: LBNL's Berkeley Accelerator Space Effects Facility (BASEF).
Energy Tune: 10 MeV
Flux: 1.2×10^4 to 1.9×10^5 particles/cm^2/s.

BASEF Ion	Incident LET (MeVcm^2/mg)
Ne	3.45
Ar	9.74
Cu	21.3
Kr	31.3
Xe	58.8

IV. Test Hardware and Software

1. DUT (Device Under Test) Description

The section of the TLK2711 tested in this test is a serializer/deserializer that converts between data formats of 16 bit parallel with clock and 8b/10b encoded serial bit stream. Serial loopback functionality is integrated, bypassing the serial output driver and input buffer when engaged. Pseudo-Random Bit Sequence (PRBS) generation and detection functionality is also integrated, allowing serial link verification when embedded within a system.

Generally there are two sections of the DUT, serialization and deserialization. The serializer is diagramed in the upper half of Figure 1. Two byte (16 bit) wide data, TXD0..TXD15, enters from the left (See Figure 1, TLK2711 Block Diagram, for the functional and signal descriptions). A latch clock for that data, TXCLK, enters below that. Between these are two signals that indicate whether each byte is to be encoded as data or as a special control signal ("K character"). These are TKLSB and TKMSB.

In usual operation, the parallel data is 8b/10b encoded and serialized into a 20-bit long serial bit stream, and is output as a differential signal with positive and negative ("P" and "N") polarities, on the upper right side of Figure 1, TXP and TXN. Note that several things are achieved in using the 20 bits to convey 16 bits of data. Ensuring sufficient clock component in the data stream is one of these things. Indicating whether each transmitted symbol is data or is a K character is another.

A frequency multiplier raises the parallel data clock, TXCLK, to the serial rate of 20 times that frequency in the "Clock Synthesizer" block below the rest of the serializer portion of the diagram. It is important to note that this synthesizer provides a *necessary* input for the lower, deserializer, portion of the DUT.

QuickTime™ and a
TIFF (Uncompressed) decompressor
are needed to see this picture.

Figure 1. TLK2711 Block Diagram (from datasheet)

The deserializer is diagrammed in the lower half of Figure 1. It is, roughly, the inverse of the serializer. Serial differential data is input on the right side inputs, RXP and RXN. This data stream is used, in conjunction with the serializer's synthesized high-speed clock to regenerate a phase-locked clock for the incoming serial data stream. The data boundaries are detected and the data is 8b/10b decoded, parallelized, and K characters are detected and flagged (by the RKLSB and RKMSB signal outputs). The data/K characters are output on the two-byte wide (RXD0..RXD15) data bus, along with the clock for that data (RXCLK).

2. DUT Assembly Description

The TLK2711 devices in RCP PowerPad™ PQFP-64 packages, delidded, were obtained mounted to evaluation assemblies (TLK2501 Serdes EVM Kit). Each assembly provided fairly complete access to all signals on both sides of the serializer and deserializer sections, both serial and parallel, including clocks and control signals. Separate power inputs for V_{dd} (digital power) and V_{ddA} (analog power) were provided. Two assemblies were used in each test, one operating the serializer portion and the other operating the deserializer portion. Because either of the assemblies could be irradiated, both are referred to as DUT assemblies, but only one was irradiated during any given test run.

3. Test Equipment Description

A GPIB-connected quad channel power supply (Agilent N6700) provided power for the deserializer (Rx) DUT assembly, the serializer (Tx) DUT assembly and provided a DC voltage to a Bias-T used in the setup (See attached block diagram in Figure 2).

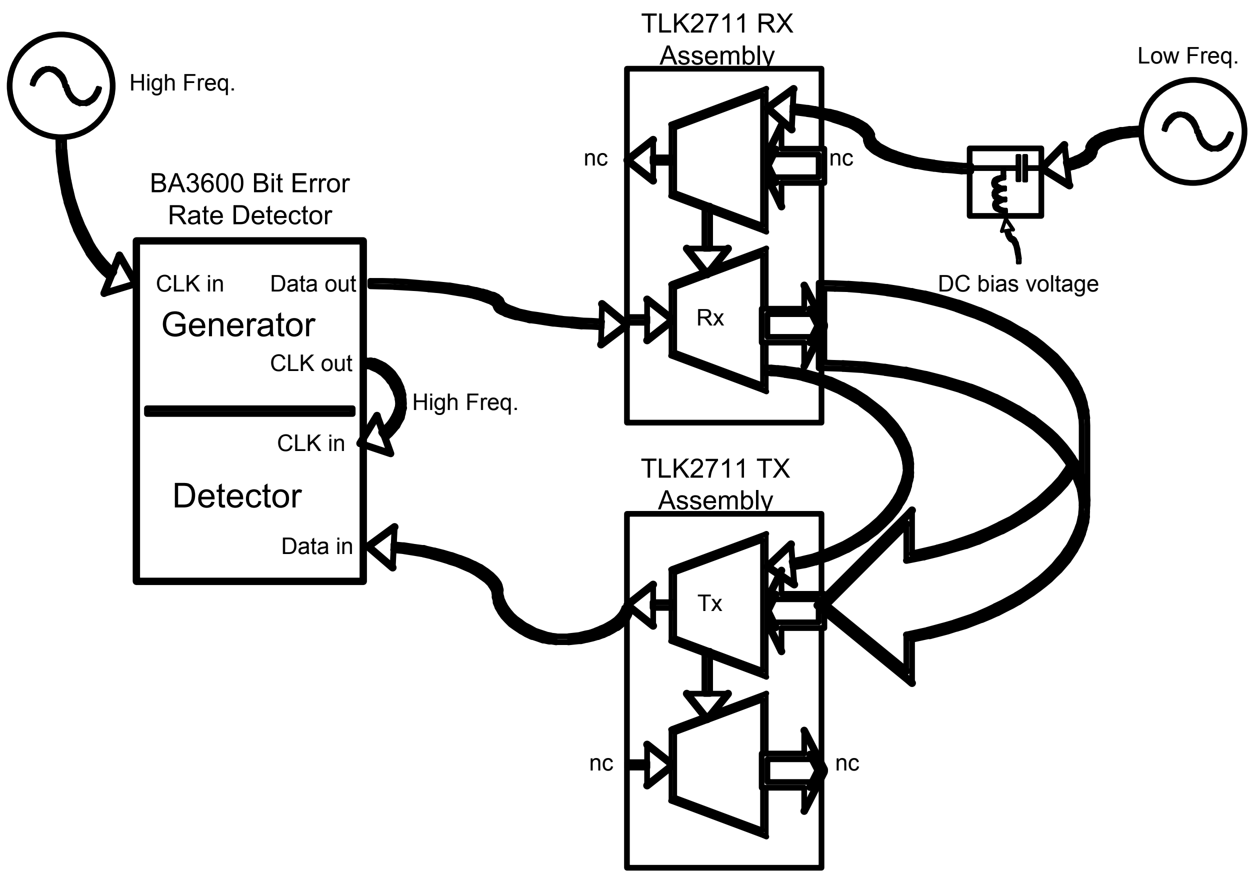

Figure 2. Test Setup Block Diagram.

Two GPIB-connected RF signal generators an HP83712B (to 20 GHz) and an HP8648C (to 3 GHz) provided frequency references for the test. These generators have standard

10 MHz reference Inputs and Outputs. In order to maintain frequency synchronization between them the HP83712B 10 MHz output was used to lock the HP8648C. Thus if one's frequency setting was twenty times the other, the actual signals would be very close or exactly twenty times apart. DUT specifications require these two frequencies to be within 100 ppm. Proper test protocol requires nominal frequency differences to not affect the test. This setup provided close to, or exactly, zero ppm difference.

The HP83712B provided frequency reference to the Bit Error Rate Detector (BERT) (described next paragraph). The HP8648C provided frequency reference to the serializer DUT's lower frequency input via a Bias-T, which allowed the addition of a DC bias voltage from the power supply to the RF signal.

Serial link data generation and detection functions were provided by a Synthesis Research BA3600 Bit Error Rate Detector (BERT). This system is functionally (though not physically) separated in two subsystems. From an external frequency reference and current settings, test signals are generated. A differential clock and a differential data stream are generated. These are fed to the DUT. The output of the DUT is fed to the second functional subsystem, the detector, of the BA3600 BERT. With a frequency reference and the incoming bit stream along with knowledge of what the data "ought" to be, the detector analyzes the data for errors. Errors are captured in their entirety and are characterized.

Bit errors can be either single or multiple, and multiple errors can be contiguous or can be separated by some number of correct bits. Testing a link with throughput of ~1 GBPS with a particle-induced event (SEE) rate of a few per second means that many thousands of bits of correct data will pass between events, even if the events result in erroneous data periods lasting many thousands of bits. The following definitions were used in this testing. A bit error is a bit that does not have the correct value. A single bit error event is a particle-induced event in which only one bit is erroneous, and which is followed by more than the defined minimum number of correct bits (in order that it be clear that following errors are not related to the same event). This quantity, the space between error events, is expressed as the Maximum Error Free Interval (MEFI), the number of correct bits beyond which a current error event is considered finished. A multiple bit error event is one in which multiple erroneous bits are all separated by less than (or equal to) an MEFI. For the purposes of this testing, where there can be a logical or organizational relationship between 20 bits, the MEFI is set to 20.

Likewise, in BER testing it is useful to be able to set the minimum number of erroneous bits (Minimum Burst Length, MBL) required to consider an event a multiple bit error event. Testing of systems that have, for example, error detection and correction able to handle any three bit errors might involve setting the MBL to four. For the purposes of this testing an MBL of 2 is appropriate and is used.

4. Test Setup

In order to look for separable radiation sensitivity information, the serializer portion of one DUT and the deserializer portion of another DUT were used in the setup (See Figure 2). A high frequency signal generator provides a CW signal at a frequency of "High Freq." to the BERT, from which the generator portion of the BERT provides a copy of the "High Freq." signal to the detector portion, and the selected serial data pattern (at a bit rate of "High Freq.") to a DUT.

The DUT with the serial data pattern input requires a low frequency ("Low Freq.") reference in order to be able to phase lock to the pattern. The "Low Freq." does not have to be frequency or phase locked, but does have to be with some limit, such as 100 ppm (0.1 MHz at a data rate of 1 GHz). To ensure this and to minimize the effects of frequency mismatch, the "Low Freq." generator is frequency-referenced to the "High Freq." generator.

With the "Low Freq." input and the high speed serial data pattern input the DUT designated "Rx" parallelizes and decodes the data. This parallel data, along with the clock and K-character flags, are passed to another DUT, designated "Tx". These signals constitute everything required for the Tx DUT to generate a serial bit stream. This serial bit stream is fed to the BERT detector for analysis.

The vagaries of 8b/10b coding along with the design of the DUT make it non-trivial to calculate a data pattern which will decode in the Rx and encode in the Tx to the identical bit sequence (a requirement for BERT operation). There is a pattern synchronization uncertainty of incurred primarily in the Rx deserialization process (from zero to 31 bit periods) although Tx serialization adds another four bit periods of uncertainty. Due to the link's variable 'latency' the detector portion of the BERT is set to auto-synchronize pattern alignment upon start of operation and every time there is an excess of errors. This is classified as a Resync error if it occurs during a test run.

V. Test Methods

For each run, the test setup was powered up and the bit stream started, allowing the BERT to synchronize. Once operating, either the transmit or receive DUT was placed in the beam line and exposed to the ion beam. For each test run, the beam fluence was allowed to reach 10^7 ions/cm^2 or the beam would be stopped if a high current condition was observed. The process was cycled through all the LET beams and both transmit and receive DUTs. During the exposure time, any error events were monitored and captured by the BERT for post processing.

VI. Results

Single Event Destructive

Two parts, biased and operating as described above, were tested with heavy ions with LETs ranging from 3.45 to 58.8 MeV-cm^2/mg, with at least 10^7 ions/cm^2 at each LET. In no test condition were any destructive conditions. Therefore, the Texas Instrument TLK2711 Transceiver is considered to have an LET threshold for destructive events of greater than 58.8 MeV-cm^2/mg.

Single Event Upsets

Upset events were observed for all test conditions. There were three types of upset events that were observed. These are the single bit error, the burst error, and the resync error. A single bit error is defined as an erroneous bit preceded by at least 20 bits of correct data and followed by at least 20 bits of correct data. Figure 3 shows the cross section versus effective LET curve for the single bit errors observed during this testing. While still close, there does appear to be a difference in the upset rate comparing the cases when either the transmit side or the receive side is the DUT in the ion beam. The plot shows the raw data (symbols), where the error bars represent one standard deviation, and the Weibul fit to the data (solid lines). The Weibul parameters for the two fits are given in the following table.

Weibul Parameter	Transmit DUT in Beam	Receive DUT in Beam
σ_{sat} (cm^2)	5.4 x 10^{-5}	3.75 x 10^{-5}
LET_0 (MeV-cm^2/mg)	1.5	1.1
W	30	16
S	2.5	2.5

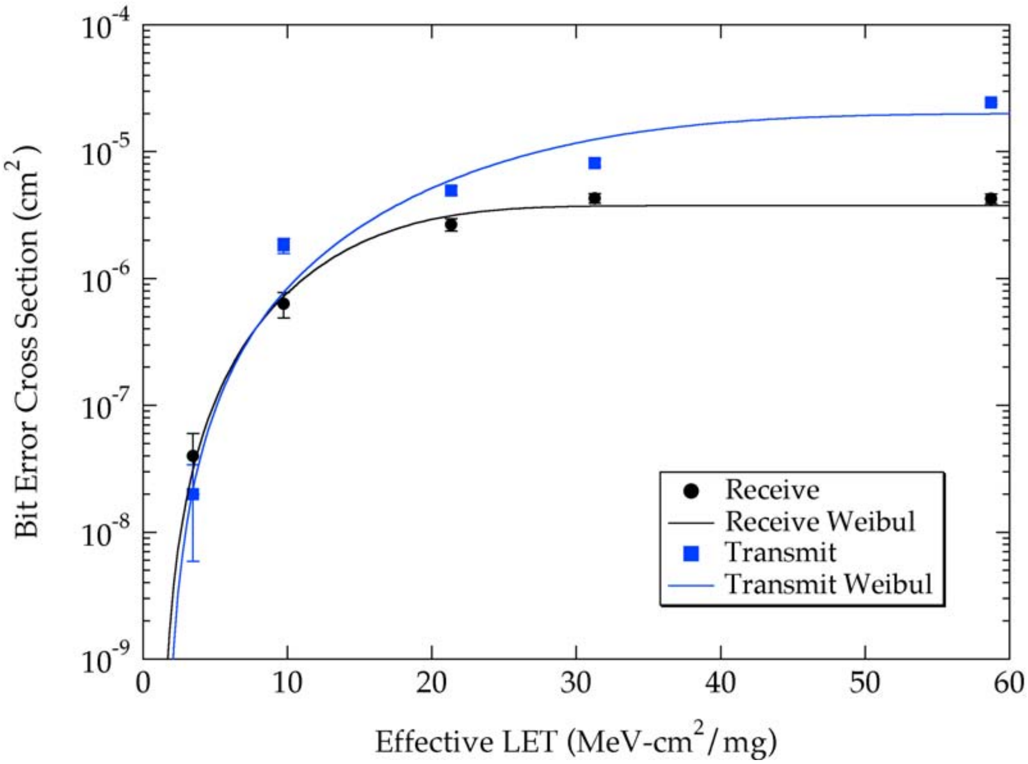

Figure 3. Single Bit Error Cross Section versus LET

A burst error is defined as an event where multiple bits are in error within 20 bits of one another. The start of a burst is at the first wrong bit that is preceded by 20 correct bits and the end of the burst is when the last bit in error is followed by 20 correct bits. The overall burst length and total number of bits in error throughout the burst are recorded by the BERT but must be processed to recover. The analysis for this report covers just that the burst events happen and their cross section calculated. Burst histograms are not part of this test report but can be made available.

Figure 4 shows the cross section versus effective LET curve for the burst errors observed during this testing. Unlike the bit error case, there does not appear to be a difference in the burst error rate comparing the cases when either the transmit side or the receive side of the DUT is in the ion beam. The plot shows the raw data (symbols), where the error bars represent one standard deviation, and the Weibul fit to the data (solid line). The Weibul parameters for the fit are given in the following table.

Weibul Parameter	Either DUT in Beam
σ_{sat} (cm^2)	5.4 x 10^{-5}
LET_0 (MeV-cm^2/mg)	2.2
W	11
S	1.7

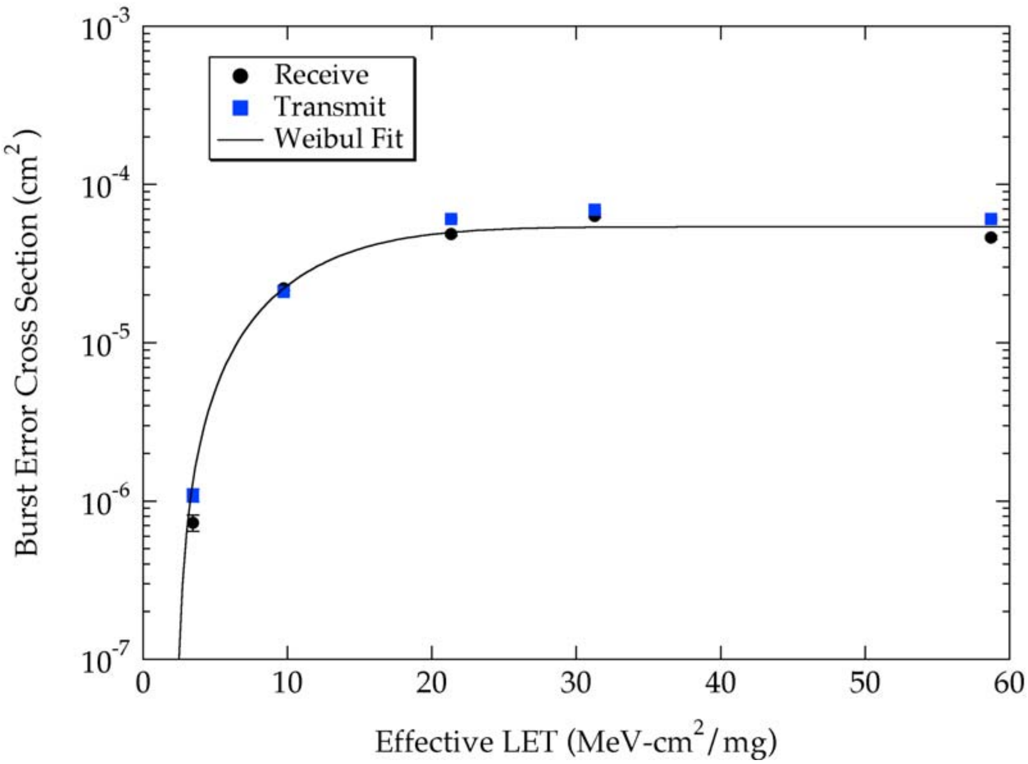

Figure 4. Burst Error Cross Section versus LET

Finally, when there are sufficient errors in succession that the BERT loses sync, the BERT issues a resync command and the event is recorded. Figure 5 shows the cross section versus effective LET curve for the resync errors observed during this testing. Again there does not appear to be a difference in the resync error for either the transmit side or the receive side of the DUT is in the ion beam. The plot shows the raw data (symbols), where the error bars represent one standard deviation, and the Weibul fit to the data (solid line). The Weibul parameters for the fit are given in the following table.

Weibul Parameter	**Either DUT in Beam**
σ_{sat}(cm^2)	1.5 x 10^{-5}
LET_0 (MeV-cm^2/mg)	1.5
W	10
S	2.5

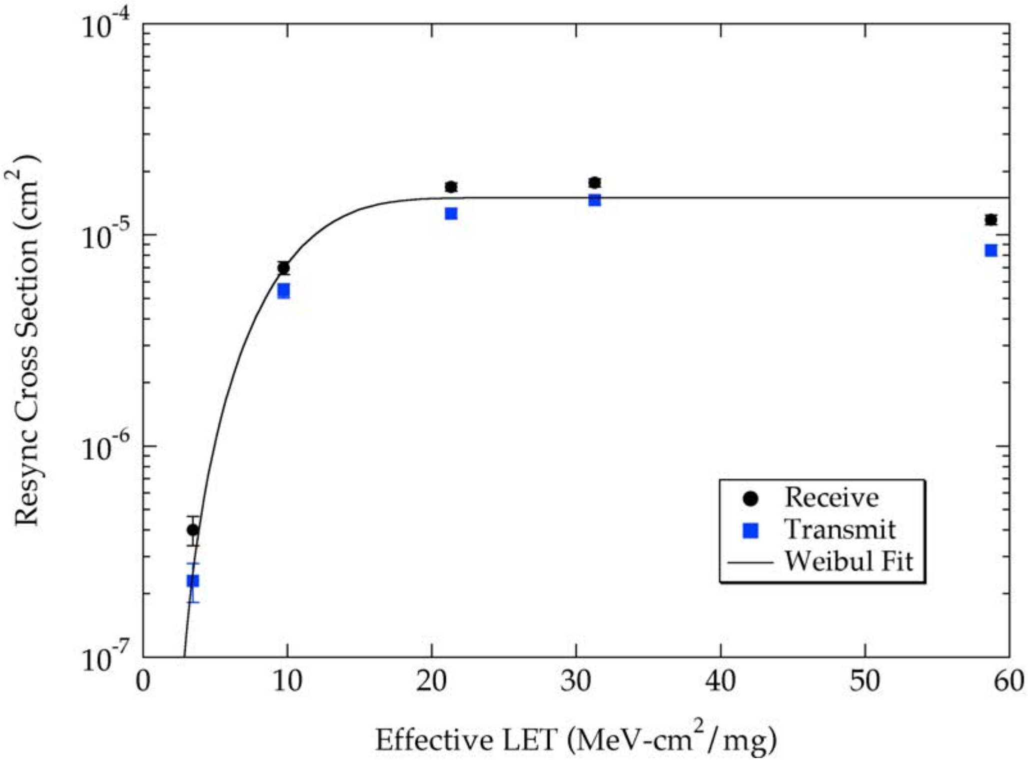

Figure 5. Resync Error Cross Section versus LET

VII. Recommendations

No destructive events were observed in the Texas Instrument TLK2711 Transceiver but if the system would be sensitive to the observed transients, then mitigation techniques would need to be employed.